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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,459	09/16/2003	Steven N. Bathiche	003797.00546	9612

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EXAMINER	
PHAM, TAMMY T	
ART UNIT	**PAPER NUMBER**
2675	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,459	BATHICHE, STEVEN N.	
	Examiner	Art Unit	
	Tammy Pham	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 7-11, 13-19 and 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Barker et al. (US Patent No: 5,675,329).

As for claim 1, Barker teaches of a computer keyboard (11), comprising:

a plurality of keys, each key of the plurality having an unpressed condition in which no force is exerted upon the key by a user and a pressed condition in which force is exerted on the key by a user in column 2, lines 34-41; and

a force detection circuit (12) configured to:

scan each key of the plurality to determine if a scanned key is in a pressed condition,

quantify, upon determining that a scanned key is in a pressed condition, the force exerted by a user on said key determined to be in a pressed condition, and

proceed, upon determining that a scanned key is not in a pressed condition, to another key of said plurality without attempting to determine a force exerted on the key determined not to be in a pressed condition in column 4, lines 12-23.

As for claim 2, Barker teaches of the computer keyboard (11) of claim 1, wherein the plurality of keys includes multiple character keys having respective characters assigned thereto and a plurality of modifier keys, and wherein the force detection circuit (12) comprises a microprocessor (18) configured to generate a first signal upon detecting a character key to be in a pressed condition and to generate a different signal upon detecting said character key and a modifier key to simultaneously be in a pressed condition in column 1, lines 28-44.

As for claim 3, Barker teaches of the computer keyboard (11) of claim 1, further comprising:

a first group of conductors;

a second group of conductors positioned in close proximity to the first group of conductors, the first and second groups of conductors forming a plurality of intersections between first group conductors and second group conductors; and

a force sensitive resistive element located between the first group conductor and the second group conductor of each of the plurality of intersections in column 2, lines 42-62. Where the magnetic and capacitive technologies are considered the conductors since they are of electrically conducting material.

each of the plurality of intersections corresponds to an associated key of the plurality of keys, each of the associated keys configured to compress the resistive element located at the corresponding intersection upon exertion of force on the associated key, and

the force detection circuit (12) is configured to determine force exerted upon each of the associated keys based upon changes in resistance value of the resistive element at each corresponding intersection in column 2, lines 42-62.

As for claim 7, Barker teaches of the computer keyboard (11) of claim 3, wherein the detection circuit comprises a microprocessor (18) and a RC network in column 2, lines 58-61.

As for claim 8, Barker teaches of a computer keyboard (11), comprising

a grid of first group conductors and second group conductors, the first and second group conductors forming a plurality of intersections;

a force-sensitive resistive element at each intersection of the plurality located between the first and second group conductor forming said intersection;

a plurality of keys located above the plurality of intersections, each key being associated with one intersection and configured to exert force on the conductors and force-sensitive resistive element of the associated intersection during a key press;

a microprocessor (18) having a plurality of first group conductor pins each in contact with one of the first group conductors and a plurality of second group conductor pins each in contact with one of the second group conductors;

a sub-circuit connected to at least one of the second group conductors, the sub-circuit having a resistor network switchable by the microprocessor (18) between a low resistance value and a high resistance value; and an Analog to Digital Converter (ADC) coupled to the sub-circuit and to the microprocessor (18) in column 2, lines 65-20.

As for claim 9, Barker teaches of the computer keyboard (11) of claim 8, wherein the microprocessor (18).

ground to an individual conductor pin,

test another conductor pin for a threshold voltage level while the resistor network is switched to the high resistance value,

switch the resistor network to the low resistance value upon detecting the threshold voltage level on the tested conductor pin, and

receive from the ADC a digital value of a voltage on the tested conductor pin while the resistor network is switched to the low resistance value in column 2, lines 55-63. Barker does not go into detail of the operations of the force detection circuit, Barker does mention that various force sensing or detection devices/circuit can be used, and therefore, includes the process as described above.

As for claim 10, Barker teaches of the computer keyboard (11) of claim 9, comprising a plurality of sub-circuits connected to a plurality of conductors of the second group of conductors in column 2, lines 55-63.

As for claim 11, Barker teaches of the computer keyboard (11) of claim 9, wherein the microprocessor (18) is configured to: store the identity of a plurality pressed keys and force values associated with the pressed keys, and generate a data message containing the identities and associated force values in column 4, lines 24-40.

As for claim 13, Barker teaches that the computer keyboard (11) of claim 9, wherein the plurality of keys includes multiple character keys having respective characters assigned thereto and a plurality of modifier keys in column 4, lines 25-40.

As for claims 14 and 21, Barker teaches of the computer keyboard (11) of claim 13, wherein the plurality of keys includes at least 36 character keys in column 2, line 52.

As for claim 15, Barker teaches that the computer keyboard (11) of claim 9, wherein the microprocessor (18) is configured to:

sequentially test each key for a key press by grounding a conductor pin connected to one of the conductors forming the associated intersection and testing for the threshold voltage level on the other of the conductors forming the associated intersection, and

receive, for only the keys for which the threshold voltage level was detected, the digital value from the ADC in column 2, lines 55-63. Barker does not go into detail of the operations of the force detection circuit, Barker does mention that various force sensing or detection devices/circuit can be used, and therefore, includes the process as described above.

As for claim 16, Barker teaches of the keyboard of claim 15, wherein the microprocessor (18) is configured to generate a data message containing identifiers for multiple keys of the plurality for which the threshold voltage level was detected and digital values from the ADC corresponding to the multiple keys in column 2, lines 63-10.

As for claim 17, Barker teaches of a microprocessor (18) having preprogrammed instructions for performing steps comprising:

placing a detection circuit in a first state in which an identity of a pressed keyboard key is determined;

placing the detection circuit in a second state in which an amount of force applied to a pressed key is measured;

scanning each key of a keyboard for pressed keys by testing each key for a key press when the detection circuit is in the first state;

measuring, when the detection circuit is in the second state and only as to pressed keys, the force applied to the pressed keys in column 4, lines 12-23.

As for claim 18, Barker teaches of the microprocessor (18) of claim 17, wherein said measuring comprises receiving a digital value for detection circuit voltage, and having additional preprogrammed instructions for performing steps comprising:

instructing an Analog to Digital Converter (ADC) to convert a detection circuit voltage to a digital value; and

reading from the ADC a digital value for the detection circuit voltage in column 2, lines 63-66.

As for claim 19, Barker teaches of the microprocessor (18) of claim 17 having additional preprogrammed instructions for performing steps comprising:

storing an identifier for multiple pressed keys;

storing force measurements for the multiple pressed keys;

generating a data message containing the stored identifiers and force measurements in column 2, lines 63-20.

As for claim 22, Barker teaches of the microprocessor (18) of claim 17 having additional preprogrammed instructions for performing steps comprising:

selecting a conductor pin from a group of conductor pins;

testing the selected conductor pin for a threshold voltage level;

upon detecting the threshold voltage level on the selected conductor pin, placing the detection circuit in the second state by altering the resistance of a resistance network; and

when in the second state, receiving a digital value for a voltage on the selected conductor pin in column 2, lines 55-63. Barker does not go into detail of the operations of the force detection circuit, Barker does mention that various force sensing or detection devices/circuit can be used, and therefore, includes the process as described above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-6, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barker et al. (US Patent No: 5,675,329) in view of Omura et al. (US Patent No: 5,349,873).

As for claim 4, Barker teaches of the computer keyboard (11) of claim 3, wherein:

the force detection circuit (12) comprises a microprocessor (18) and of a first condition when scanning each key of the plurality to determine if a scanned key is in a pressed condition and in a second condition when quantifying the force exerted by a user on a key determined to be in a pressed condition in column 4, lines 10-25.

But Barker does not teach of using a voltage divider in the force detection circuit.

Omura teaches of using a voltage divider in the force detection circuit in column 9, lines 22-30.

It would have been obvious to one with ordinary skills in the art at the time the invention was made to replace the force detection circuit as taught of Barker with the force detection circuit including a voltage divider as taught by Omura, in order to measure the force through the circuitry (see Omura: column 9, line 28).

As for claim 5, Barker teaches and of the computer keyboard (11) of claim 4, wherein:

when the force detection circuit (12) is in the first condition, voltage at the voltage measuring node varies within a first range as a key is pressed,

when the force detection circuit (12) is in the second condition, voltage at the voltage measuring node varies within a second range as a key is pressed, and

the second range is larger than the first range in column 4, lines 10-25.

Omura teaches of the voltage divider includes a voltage measuring node in column 9, lines 22-30.

As for claim 6, Barker teaches of the computer keyboard (11) of claim 4, further comprising an Analog to Digital Converter (ADC), and wherein:

the microprocessor (18) determines a scanned key is in a pressed condition when voltage on a tested conductor of the corresponding intersection reaches a threshold value, and

the microprocessor (18), after determining the scanned key is in a pressed condition, instructs the ADC to output a digital value of a voltage on the tested conductor in column 2, lines 65-20.

As for claims 12 and 20, Barker teaches of computer keyboard (11) of claim 11, wherein the microprocessor (18) is configured to generate the data message in column 4, lines 25-40.

Barker does not teach that the data message is in the form of a Human Interface Device (HID) report.

Applicant has not disclosed any specific advantage or criticality to using the HID. As such, the data message in the form of HID is an obvious matter of design choice.

Therefore, it would have been obvious to generate the data message in the form of HID, since any form would perform equally well at transmitting data to and from the microprocessor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tammy Pham
January 26, 2006

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SUPERVISORY PATENT EXAMINER